

JEFFERSON COLLEGE

COURSE SYLLABUS

ETC255

INTRODUCTION TO DIGITAL CIRCUITS

6 Credit Hours

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Revised Date: August, 2007
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JEFFERSON COLLEGE

Hillsboro, Missouri

I. Course Description

Title: ETC255 Introduction to Digital Circuits

Curriculum: Electronics Technology

Semester Hours: 6

Prerequisite: ETC133 Semiconductors II

Catalog Description: Introduction to Digital Circuits will involve a study of basic logic circuit design and specific operating characteristics of commonly used integrated circuit technologies. Sequential and combinational logic circuits are developed, implemented, and analyzed in detail.

II. Expected Learning Outcomes with Assessment Measures

Upon Completion of this course, the student will be able to:

1. Demonstrate ability to represent basic logic gates using standard Mil. Spec. positive and negative logic symbology and ANSI/IEEE std. 91-1984 logic symbology. *(Evaluate by written exams, quizzes)*
2. Demonstrate knowledge and understanding of the truth tables for the basic logic gates. *(Evaluate by written exams, quizzes)*
3. Demonstrate ability to write, reduce, and implement Boolean expressions. *(Evaluate by written exams, quizzes)*
4. Demonstrate knowledge and understanding of the static and dynamic characteristics of the basic logic families including TTL, CMOS, and ECL. *(Evaluate by written exams, quizzes and observation of lab performance)*
5. Demonstrate ability to represent numbers and perform basic arithmetic operations using binary, octal, hexadecimal, numbering systems, and 8421 BCD and XS3 BCD codes. *(Evaluate by written exams, quizzes and observation of lab performance)*
6. Demonstrate knowledge and understanding of gray code, information codes, and error detection and correction schemes. *(Evaluate by written exams, quizzes)*
7. Demonstrate knowledge and understanding of basic digital devices such as encoders, decoders, multiplexers, demultiplexers, astable, monostable, and bistable multivibrators, latches, display devices, display drivers, counters, shift registers, and arithmetic circuits. *(Evaluate by written exams, quizzes and observation of lab performance)*
8. Demonstrate skill in constructing digital circuits from a logic diagram. *(Evaluate by observation of lab performance)*
9. Demonstrate ability to successfully analyze and troubleshoot basic asynchronous and synchronous logic devices and circuits. *(Evaluate by written exams, quizzes and observation of lab performance)*

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III. Course Outline

Unit: 1

Lesson: 1

Title: Numbering Systems and Codes

Objectives: Upon completion of the lesson, you should be able to, by written examination:

1. express whole and fractional numbers in the binary, octal, and hexadecimal numbering system,
2. convert whole and fractional numbers between the decimal, binary, octal, and hexadecimal numbering systems,
3. state the rules for binary addition and subtraction,
4. express the *1's and 2's complement* of binary and hexadecimal numbers,
5. perform binary subtraction using 1's and 2's complement arithmetic,
6. perform binary multiplication and division,
7. state the definition of the term *Binary Coded Decimal (BCD) Code*,
8. convert decimal to *8421 BCD (NBCD)* and vice versa,
9. perform BCD addition,
10. *express the *9's and 10's complement* of NBCD values,
11. *perform NBCD subtraction using 10's complement arithmetic,
12. *convert decimal to *BCD Excess-3* and vice versa,
13. *perform BCD Excess-3 addition and subtraction,
14. convert binary to *Gray code* and vice versa.

Reading Assignment: Floyd, Digital Fundamentals, 9th edition, pp. 46-102

Problems Assignment: pp. 104-108

5,7,9,13,14,15,17,19,23,25,29,31,35,37,39,47,51,55,59

Laboratory: None

Interactive Computer Software:

1. MicaSOFT Electronics and Microelectronics Tutor

M3: 1. Binary adders

2. DrillMAKER, Coastal Computer Company

Exercise: 1, 2, 3, 4, 5, 6, 7, 17, 18, 19, 20

Problems per exercise: 3

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Unit: 2

Lesson: 1

Title: Digital Logic Circuits

Objectives: Upon completion of the lesson, you should be able to, by written examination:

1. state the definition of the terms:
 - a. *positive logic*,
 - b. *negative logic*,
2. state the definition of the terms:
 - a. *rise time of a pulse*,
 - b. *fall time of a pulse*,
 - c. *pulse width of a pulse*,
 - d. *pulse repetition frequency of a pulse*,
 - e. *duty cycle of a pulse*,
3. by direct measurement:
 - a. determine the rise time of a pulse,
 - b. determine the fall time of a pulse,
 - c. determine the pulse width of a pulse,
 - d. determine the pulse repetition frequency of a pulse,
 - e. determine the duty cycle of a pulse,
4. *describe the pulse distortion produced by an *over damped* and *under damped* series LCR circuit,
5. *determine the value of resistance required to *critically damp* a series LCR circuit,
6. state the definition of the term *truth table*,
7. state the truth table and draw the logic symbol for a *logic inverter (NOT)*,
8. state the truth table and draw the logic symbol for an *N-input AND gate*,
9. state the truth table and draw the logic symbol for an *N-input OR gate*,
10. state the truth table and draw the logic symbol for an *N-input NAND gate*,
11. state the truth table and draw the logic symbol for an *N-input NOR gate*,
12. draw the *negative logic symbol (logic dual)* for a/an:
 - a. AND gate,
 - b. OR gate,
 - c. NAND gate,
 - d. NOR gate,
 - e. logic inverter (NOT),
13. draw the logic symbol for the *Exclusive OR gate*,
14. state the truth table for the *Exclusive OR gate*,
15. draw the logic symbol for the *Exclusive NOR gate*,
16. state the truth table for the *Exclusive NOR gate*,
17. state the definition of the terms:
 - a. **fan-in*,

b. *fan-out*,

Reading Assignment: Floyd, Digital Fundamentals, 9th edition, pp. 1-40, 112-168

Problems Assignment: pp. 42-44

3,5,6,7,9,11,19

Problems Assignment: pp. 170-173

1,3,5,7,9,11,13,14,15,17,19,21,

Laboratory: Buchla, Experiments in Digital Fundamentals, 9th edition

Experiment 4: Logic Gates

Steps of Procedure: 1, 2, 3, 4, 5, 6,

For Further Investigation:

Questions for Experiment 4: 1, 2, 3, 4, 5, 6

Supplemental Experiment: Series LCR Transient Response

Interactive Computer Software:

1. MicaSOFT Electronics and Microelectronics Tutor

M3: Boolean Algebra and Logic Gates

2. LogicMAKER, Coastal Computer Company

Exercise: 1, 2, 3, 4, 5, 15, 16

Problems per exercise: 3

SUPPLEMENTAL LABORATORY

ETM155

Introduction to Digital Circuits

Unit: 2

Lesson: 1

Title: Series LCR Transient Response

Objectives: Upon completion of the laboratory, you should be able to, by demonstration and written examination:

1. observe the output of a series LCR circuit with a pulse waveform at the input:
 - a. *over damped*,
 - b. *critically damped*,
 - c. *under damped*,
2. given the value of the circuit capacitance and inductance, calculate the value of circuit resistance required to critically damp a series LCR circuit.

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Unit: 3

Lesson: 1

Title: Digital Device Families

Objectives: Upon completion of the lesson, you should be able to, by written examination:

1. state the definition for *SSI*, *MSI*, and *LSI* integrated circuit classifications, pp.30
2. state the definition of the terms:
 - a. *current sink*,
 - b. *current source*,
3. *schematically represent a *bipolar saturated switch logic inverter*,
4. *given the electrical characteristics of the load, design a bipolar saturated switch logic inverter,
5. state the advantage of *non-saturated bipolar switching circuits*,
6. state the electrical characteristics of standard TTL (74 series) devices:
 - a. *high level input and output current*,
 - b. *low level input and output current*,
 - c. *high level input and output voltage*,
 - d. *low level input and output voltage*,
 - e. *noise immunity*,
 - f. *propagation delay*,
 - g. *power supply requirements*,
7. *describe the power supply *decoupling* requirements for TTL devices,
8. describe the characteristics and operating requirements for *totem-pole* and *open collector* TTL gates,
9. write the output expression for *wire ANDed* open-collector TTL gates,
10. describe the input characteristics and principal application of *Schmitt trigger* TTL gates,
11. describe the output characteristics of gates with *tri-state (three-state) outputs*,
12. describe the relative characteristics of the TTL subfamilies:
 - a. *high speed*,
 - b. *low power*,
 - c. *Schottky-clamped*,
 - d. *low power Schottky*,
 - e. *advanced Schottky*,
 - f. *advanced low power Schottky*,
13. draw the schematic symbol for the N-channel and P-channel enhancement mode transistor (E MOSFET),
14. state the input impedance characteristic of E MOSFET's,
15. state the gate-to-source voltage (V_{gs}) requirement to turn on or off an N-channel or P-channel E MOSFET,

16. describe the construction of MOS logic gates,
 - a. classification:
 1. NMOS,
 2. PMOS,
 - b. logic inverter (NOT),
 - c. NAND,
 - d. NOR,
17. schematically represent the *CMOS logic inverter (NOT)*,
18. describe the electrical characteristics of CMOS gates,
 - a. *high level input and output current*,
 - b. *low level input and output current*,
 - c. *high level input and output voltage*,
 - d. *low level input and output voltage*,
 - e. *noise immunity*,
 - f. *propagation delay*,
 - g. *power supply requirements*,
19. describe the precautions for handling CMOS and MOS devices,
20. *state the TTL compatibility of *buffered-B series CMOS gates*,
21. *state the definition of the term *level shifting* as applied to logic interfacing,
22. *describe the characteristics of *CMOS analog transmission gates (bilateral switch)*:
 - a. *on resistance*,
 - b. *off resistance*,
23. describe the electrical characteristics of *emitter-coupled logic (ECL)*:
 - a. *propagation delay*,
 - b. *logic voltage levels*,
 - c. *power supply requirements*.
24. determine the effects of a pulse driving a:
 - a. non-terminated transmission line,
 - b. terminated transmission line,
25. measure the length of an open transmission line by measuring the flight time of a reflected pulse.

Reading Assignment: Floyd, Digital Fundamentals, 9th edition, pp. 784-817

Problems Assignment: pp. 818-823

1,3,5,7,9,11,13,16,17,19,25,27,29

Laboratory: Buchla, Experiments in Digital Fundamentals, 9th edition

Experiment 6: Interpreting Manufacturer's Data Sheets

Steps of Procedure: 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16

For Further Investigation: 1, 2, 3, 4

Questions for Experiment 6: 1, 2, 3, 4, 5

Supplemental Experiment:

1. Pulse Transmission
2. Transistor Switching

Interactive Computer Software: LogicMAKER, Coastal Computer Company

Exercise: 28

Problems per exercise: 3

SUPPLEMENTAL LABORATORY

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Introduction to Digital Circuits

Unit: 3

Lesson: 1

Title: Pulse Transmission

Objectives: Upon completion of the laboratory, you should be able to, by demonstration and written examination:

1. determine the effects of a pulse driving a:
 - a. non-terminated transmission line,
 - b. terminated transmission line,
2. measure the length of an open transmission line by measuring the flight time of a reflected pulse.

SUPPLEMENTAL LABORATORY

ETM255

Introduction to Digital Circuits

Unit: 3

Lesson: 1

Title: Transistor Switching

Objectives: Upon completion of the laboratory, you should be able to, by demonstration and written examination:

1. measure bipolar transistor:
 - a. *turn-on time*,
 - b. *storage time*,
 - c. *turn-off time*,
2. determine the relationship between bipolar transistor saturation collector current and storage time,
3. observe the operation of a base *speed-up* capacitor,
4. compare saturated and non-saturated bipolar switches.

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Unit: 4

Lesson: 1

Title: Reduction and Implementation of Boolean Expressions

Objectives: Upon completion of the lesson, you should be able to, by written examination:

1. write the Boolean expression for a logic inverter,
2. state the *laws of complementation*,
3. write the Boolean expression for an AND gate,
4. state the *AND laws*,
5. write the Boolean expression for an OR gate,
6. state the *OR laws*,
7. write the Boolean expression for a NAND gate,
8. construct a logic inverter from a NAND gate,
9. construct an AND gate from a NAND gate,
10. construct an OR gate from a NAND gate,
11. write the Boolean expression for a NOR gate,
12. construct a logic inverter from a NOR gate,
13. construct an OR gate from a NOR gate,
14. construct an AND gate from a NOR gate,
15. apply the laws of Boolean algebra for the simplification and implementation of Boolean expressions:
 - a. *AND laws*,
 - b. *OR laws*,
 - c. *laws of complementation*,
 - d. *DeMorgan's laws*,
 - e. *commutative laws*,
 - f. *distributive laws*,
 - g. *associative laws*,
 - h. *laws of absorption*,
16. write the Boolean expression for a truth table as:
 - a. a *sum-of-minterms*,
 - b. a *product-of-maxterms*,
17. transform a sum-of-minterm form Boolean expression to a product-of-maxterm form and vice versa,
18. given the truth table of up to five variables:
 - a. reduce the Boolean expression by the application of *Karnaugh mapping* techniques:
 1. *minterm reduction*,
 2. *maxterm reduction*,
 - b. implement the result of the reduction process in *AND/OR/invert, NAND*, or

NOR logic,

19.map and reduce incompletely specified functions,

20.apply the techniques of *multiple output minimization*,

21.state the truth table and draw the logic symbol for the Exclusive OR and Exclusive NOR gate,

22.write the Boolean expression for the *Exclusive OR* and *Exclusive NOR* gate,

23.demonstrate ability to troubleshoot logic gate networks.

Reading Assignment: Floyd, Digital Fundamentals, 9th edition, pp. 182-234, 244-282

Problems Assignment: pp. 236-240

1,3,5,7,9,11,13,15,17,19,29,31,33,39,41,43,45,47,49,51

Problems Assignment: pp. 284-289

3,5,9,11,13,15,17,19,21,23,25,27,29,31,33,35,37

Laboratory: Buchla, Experiments in Digital Fundamentals, 9th edition

Experiment 7: Boolean Laws and DeMorgan's Theorem

Steps of Procedure: 1, 2, 3, 4, 5, 6,

For Further Investigation: 1, 2

Questions for Experiment 7: 1, 2, 3, 4, 5, 6

Experiment 8: Logic Circuit Simplification

Steps of Procedure: 1, 2, 3, 4, 5, 6, 7

For Further Investigation: 1, 2, 3

Questions for Experiment 8: 1, 2, 3, 4, 5, 6

Experiment 9: The Perfect Pencil Machine (Required lab report)

Interactive Computer Software:

1. LogicMAKER, Coastal Computer Company

Exercise: 8

Problems per exercise: 3

Design Project: 9, 10, 11, 12, 13

2. DrillMAKER, Coastal Computer Company

Exercise: 9, 10, 11, 12, 13, 14, 15, 16

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Unit: 5

Lesson: 1

Title: Arithmetic, Data Control and Programmable Logic Circuits

Objectives: Upon completion of the lesson, you should be able to, by written examination:

1. state the difference between a *half-adder* and a *full adder*,
2. write the truth table for a full adder,
3. with reference to parallel addition, state the definition of the terms:
 - a. *ripple carry*,
 - b. *look ahead carry*,
4. state the basic function of a *comparator*,
5. resolve the outputs of a comparator in terms of its inputs,
6. state the definition of the term *encoder*,
7. resolve the outputs of an encoder in terms of its inputs,
8. distinguish between a *non-priority encoder* and a *priority encoder*,
9. state the definition of the term *decoder*,
10. resolve the outputs of a decoder in terms of its inputs,
11. state the driver requirements for the *common anode* and *common cathode seven segment* LED displays,
12. given the electrical specifications for the display, calculate the required current limiting resistance for the display segments,
13. state the function of a *latch input* for a seven segment decoder/driver,
14. state the function of a *ripple-blanking input* for a seven segment decoder/driver,
15. state the function of a *lamp-test input* for a seven segment decoder/driver,
16. state the definition of the term *multiplexer*,
17. apply the digital multiplexer for:
 - a. directly implementing combinational logic,
 - b. folding the multiplexer for implementing combinational logic,
18. state the definition of the term *demultiplexer*,
19. resolve the outputs of a demultiplexer in terms of its inputs,
20. describe the relationship between the decoder and the demultiplexer,
21. state the function of the *parity bit* in a binary word,
22. given a binary word, state the value of the included parity bit for:
 - a. *even parity*,
 - b. *odd parity*,
23. describe the *Programmable Logic Device (PLD)* as a component for logic implementation,
24. implement combinational logic using a programmable logic device
25. describe the use of *Read Only Memory (ROM)* as a component for logic implementation,
26. implement combinational logic using an *Erasable Programmable Read Only Memory (EPROM)*.

Reading Assignment: Floyd, Digital Fundamentals, 9th edition, pp. 22 -27, 143-150, 296-353,

536-578, 604-614

Problems Assignment: pp. 173

23

Problems Assignment: pp. 356-363

1,3,5,9,11,13,15,17,19,21,23,25,31

Problems Assignment: pp. 597-600

2, 11, 19

Problems Assignment: pp. 681-682

1,

Laboratory: Buchla, Experiments in Digital Fundamentals, 9th edition

Experiment 11: Adder and Magnitude Comparator

Steps of Procedure: 1, 2

For Further Investigation: 1, 2, 3, 4

Questions for Experiment 11: 1, 2, 3, 4, 5, 6

Experiment 12: Combinational Logic Using Multiplexers

Steps of Procedure: 1, 2, 3

For Further Investigation: 1, 2

Questions for Experiment 12: 1, 2, 3, 4, 5, 6

Experiment 13: Combinational Logic Using Demultiplexers

Steps of Procedure: 1, 2, 3, 4

For Further Investigation

Questions For Experiment 13: 1, 2, 3, 4, 5, 6

Interactive Computer Software:

1. MicaSOFT Electronics and Microelectronics Tutor

M3: 1. Binary Adders
2. Encoders and Decoders

2. LogicMAKER, Coastal Computer Company

Exercise: 48, 52, 55, 56, 57, 58, 59, 60, 62, 64, 65, 67, 68
Problems per exercise: 3

3. DrillMAKER, Coastal Computer Company

Exercise: 8
Problems per exercise: 3

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Introduction to Digital Circuits

Unit: 6

Lesson: 1

Title: Multivibrators and Latches

Objectives: Upon completion of the lesson, you should be able to, by written examination:

1. state the definition of the term *synchronous logic*,
2. state the definition of the term *asynchronous logic*,
3. state the truth table for a *NAND RS flip-flop*,
4. state the truth table for a *NOR RS flip-flop*,
5. schematically represent the NAND and NOR RS flip-flop,
6. state the truth table for the *clocked RS flip-flop*,
7. differentiate between *edge* and *pulse triggered clock inputs*,
8. state the truth table for the *synchronous inputs* of a *D-type flip-flop*,
9. state the definition of the term *transparent* as it applies to latches,
10. state the truth table for the *synchronous inputs* of a *JK-type flip-flop*,
11. state the clock requirements for a *master/slave JK-type flip-flop*,
12. contrast the *data lock-out flip-flop* and the pulse triggered master-slave JK,
13. show the construction of the *T-type* and *D-type flip-flop* from the *JK-type flip-flop*,
14. state the truth table for the *asynchronous inputs* of the T-type, D-type, and JK-type flip-flop,
15. identify the *logic assertions* made by the schematic representation of the synchronous and/or asynchronous inputs of the:
 - a. RS flip-flop,
 - b. clocked RS flip-flop,
 - c. T-type flip-flop,
 - d. D-type flip-flop,
 - e. JK-type flip-flop.
 - f. data lock-out flip-flop,
16. state the definition of the following terms:
 - a. *propagation delay time*,
 - b. *set-up time*,
 - c. *hold time*,
17. state the definition of the term *astable multivibrator*,
18. design and implement the CMOS astable multivibrator,
19. describe the principal theory of operation of the *logic ring oscillator*,
20. state the definition of the term *monostable multivibrator*,
21. describe the principal theory of operation of an IC form monostable multivibrator,
22. describe the relative advantage of a *Schmitt trigger input* over an edge trigger input for triggering a monostable multivibrator,
23. state the relative advantage of a *retriggerable* monostable multivibrator over a *non-retriggerable* monostable multivibrator,

24. given the trigger requirements, pulse width, and time between the triggers, sketch the Q output waveform of a:
- non-retriggerable monostable multivibrator,
 - retriggerable monostable multivibrator,
25. given the pulse width and the time between the triggers, calculate the *duty cycle* of a monostable multivibrator,
26. describe the principal theory of operation of the 555 IC timer in a:
- monostable mode,
 - astable mode,
27. calculate the pulse width of a 555 IC timer in a monostable mode,
28. calculate the output period of a 555 IC timer in an astable mode,
29. calculate the duty cycle of a 555 IC timer in a:
- monostable mode,
 - astable mode,
30. describe the principle theory of operation of diode modification for 50% duty cycle at the output of a 555 IC timer in an astable mode.

Reading Assignment: Floyd, Digital Fundamentals, 9th edition, pp. 370-413

Problems Assignment: pp. 415-423

1,3,5,7,9,11,13,15,17,19,21,23,29,31,35,37,41

Laboratory: Buchla, Experiments in Digital Fundamentals, 9th edition

Experiment 14: The D Latch and D Flip-Flop

Steps of Procedure: 1, 2, 3, 4, 5, 6, 7, 8, 9, 10

Questions for Experiment 14: 1, 2, 3, 4, 5, 6

Experiment 16: The JK Flip-Flop

Steps of Procedure: 1, 2, 3, 4,

For Further Investigation: 1, 2, 3

Questions for Experiment 16: 1, 2, 3, 4, 5, 6

Experiment 17: One-Shots and Astable Multivibrators

Steps of Procedure: 1, 2, 3, 4, 5

Questions for Experiment 17: 1, 2, 3

Supplemental Experiment: 555 IC Timer

Interactive Computer Software:

1. MicaSOFT Electronics and Microelectronics Tutor

M3: 1. Flip-Flops
2. Relaxation Oscillators

2. LogicMAKER, Coastal Computer Company

Exercise: 18, 20, 21, 23, 24, 25, 49, 50
Problems per exercise: 3

SUPPLEMENTAL LABORATORY

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Introduction to Digital Circuits

Unit: 6

Lesson: 1

Title: 555 IC Timer

Objectives: Upon completion of the laboratory, you should be able to, by demonstration and written examination:

1. describe the principal theory of operation of the 555 IC timer in a:
 - a. monostable mode,
 - b. astable mode,
2. calculate the pulse width of a 555 IC timer in a monostable mode,
3. calculate the output period of a 555 IC timer in an astable mode,
4. calculate the duty cycle of a 555 IC timer in a:
 - a. monostable mode,
 - b. astable mode,
5. describe the principle theory of operation of diode modification for 50% duty cycle at the output of a 555 IC timer in an astable mode.

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Unit: 7

Lesson: 1

Title: Binary Counters

Objectives: Upon completion of the lesson, you should be able to, by written examination:

1. state the definition of the term *modulus*,
2. state the relationship between the natural modulus of a binary counter and the number of stages,
3. state the basic component of the *ripple counter*,
4. state the three factors which govern whether a ripple counter will count up or down,
5. draw a modulo-N:
 - a. up-counter,
 - b. down-counter,
6. state two principal disadvantages of the ripple counter,
7. design and implement the necessary reset/preset logic to shorten the modulus of a/an:
 - a. up-counter,
 - b. down-counter,
8. determine the effective modulus of *cascaded* binary counters,
9. state two principal advantages of the *synchronous counter*,
10. using JK-type flip-flops, design and implement a:
 - a. *sequential synchronous counter*,
 - b. *non-sequential synchronous counter*.

Reading Assignment: Floyd, Digital Fundamentals, 9th edition, pp. 426-480

Problems Assignment: pp. 481-487

1,3,5,9,11,13,15,17,21,23,25,31,33,35,37

Laboratory: Buchla, Experiments in Digital Fundamentals, 9th edition

Experiment 18: Asynchronous Counters

Steps of Procedure: 1, 2, 3, 4, 5, 6, 7, 8

For Further Investigation: Design Problem

Questions for Experiment 18: 1, 2, 3, 4, 5, 6

Experiment 19: Analysis of Synchronous Counters with Decoding

Steps of Procedure: 1, 2, 3, 4, 5, 6, 7

For Further Investigation

Questions for Experiment 19: 1, 2, 3, 4, 5

Experiment 20: Design of Synchronous Counters

Steps of Procedure: 1, 2, 3

For Further Investigation:

Questions for Experiment 20: 1, 2, 3, 4, 5, 6

Interactive Computer Software: LogicMAKER, Coastal Computer Company

Exercise: 30, 34, 35, 36, 42

Problems per exercise: 3

Design Project: 37, 38

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Unit: 8

Lesson: 1

Title: Shift Registers, Shift Counters, and Microprocessors

Objectives: Upon completion of the lesson, you should be able to, by written examination:

1. state the four possible data conversions of a shift register,
2. state the number of clock pulses required to:
 - a. serially load an N-bit shift register,
 - b. serially un-load an N-bit shift register,
 - c. serially make data available from an N-bit shift register,
3. state the definition of the term *synchronous parallel loading* of a shift register,
4. state the definition of the term *preset-only parallel loading* of a shift register,
5. state the procedure for preset-only parallel loading of a shift register,
6. design and implement an N-bit *ring counter*,
7. state the relationship between the number of stages and the modulus of an N-bit ring counter,
8. design and implement an N-bit *self-correcting* ring counter:
 - a. 1's circulating,
 - b. zero circulating,
9. design and implement an N-bit:
 - a. *even modulus Johnson (shift) counter*,
 - b. *odd modulus Johnson (shift) counter*,
10. state the relationship between the number of stages and the modulus of an even modulus Johnson (shift) counter,
11. state the principal use of a Johnson (shift) counter,
12. state at least three common applications of the shift register,
13. state the clock requirements of the *dynamic MOS shift register*,
14. describe the basic design of the microprocessor,
15. state the three basic buses in a microprocessor and explain what each is used for,
16. state several applications of a microprocessor,
17. state the types of signals that would be present on the microprocessor buses.

Reading Assignment: Floyd, Digital Fundamentals, 9th edition, pp. 492-527, 692-722

Problems Assignment: pp. 528-533

1,3,5,7,9,11,13,15,17,19,23,27,31,35

Laboratory: Buchla, Experiments in Digital Fundamentals, 9th edition

Experiment 22: Shift Register Counters

Steps of Procedure: 1, 2, 3, 4, 5,

For Further Investigation

Questions for Experiment 22: 1, 2, 3, 4, 5, 6

Interactive Computer Software: LogicMAKER, Coastal Computer Company

Exercise: 29, 40, 41, 43, 44, 45, 46

Problems per exercise: 3

IV. Methods of Instruction: Lecture, Demonstration, Labs, Discussion, Computer software usage

V. Required Textbook

1. Floyd, Digital Fundamentals, 9th edition
2. Buchla, Experiments in Digital Fundamentals, 9th edition

VI. Required Materials

1. Student Version: LogicMAKER, Coastal Computer Company
2. Student Version: DrillMAKER, Coastal Computer Company
3. Electronic calculator
4. needle-nose pliers
5. wire strippers (22 ga.) optional

VII. Supplemental References

MiacSoft Computer tutorial software

VIII. Methods of Evaluation

A. Distribution of the Final Grade:

60% - Theory (tests, quizzes, homework)

30% - Laboratory (observing work habits, safety habits, homework, follow verbal instructions and perform the exercises assigned)

10% - Instructor evaluation of observed traits and characteristics

B. Assignment of Final Letter Grade:

- A - 90 to 100%
- B - 80 to 89%
- C - 70 to 79%
- D - 65 to 69%
- F - Below 65%

IX. ADA Statement

Any student requiring special accommodations should inform the instructor and the Coordinator of Disability Support Services (Library; phone 636-797-3000, ext. 169).

X. Academic Honesty Statement

As a student in the Electronics Department, you are advised of the Statement of Academic Honesty published in the Jefferson College Student Handbook. Plagiarism, Cheating, and Computer misuse violate the College's standards of academic honesty, and the expectations for conduct in the Electronics Department. Conduct related to assignments, examinations, or computer usage during the completion of assignments or examinations in violation of the standards of academic honesty may result in a failing (F) grade given for the assignment or examination, and potentially, the course.